IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Robert D. Norman	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
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Title:	SYSTEM AND METHOD FOR ASSIGNING ADDRESSES TO MEMORY DEVICES	

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE SPECIFICATION

On page 1, under the title, please insert -- This application is a Continuation of U.S. Serial No. 08/842030 filed on April 23, 1997.--

IN THE CLAIMS

Please cancel claims 4-24, 26-46, 48-54, 60, 62, and 63. Claims 1-3, 25, 47, 55-59 and 61 are now pending in this application.

1. (Once amended) A memory system comprising:

a plurality of memory devices, with each memory device comprising

(a) an array of memory cells;

(b) an addressing circuitry [adapted to address] operatively coupled to the array of the memory cells, wherein the addressing circuitry is capable of providing addresses to the array of memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus interface, including an address assign command; and

(e) a local address storage circuitry which stores a local address for identifying the storage circuitry's single [the] associated memory device once the address assign command is decoded by the command decoder;

and

a memory controller having a controller bus interface coupled to the memory device bus interface [of the memory device], with the memory controller providing the local address to be stored in the local address storage circuitry of the memory device of the memory system together with the address assign command.

2. (Once amended) The memory system of claim 1, wherein the controller bus interface of the memory controller is coupled to the memory device bus interface of the memory device by a system bus.

3. The memory system of claim 2, including a plurality of the memory devices wherein the memory controller transfers the local address to the memory devices over the system bus and the address assign command over the system bus.

25. (Once amended) A memory system comprising:

a system bus which includes a tag bus and a data bus;

a memory controller coupled to the system bus at a controller bus interface;

a plurality of memory devices, with each of the memory devices including:

an array of memory cells;

a local address storage circuitry coupled to the data bus which stores a local address for identifying the storage circuitry's single [the] associated memory device, the local address originating from the memory controller;

a comparator coupled to the data bus which compares [an] a data address on the data bus originating from the memory controller with the local address stored in the local address circuitry; and

a command decoder coupled to the tag bus which decodes commands originating from the memory controller, including commands to perform memory read operations on the memory device.

47. (Once amended) A method of controlling the operation of a memory system that includes a plurality of memory devices connected to a common system bus, with each of the memory devices including an array of memory cells and addressing circuitry which is used to uniquely address the addressing circuitry's single [address the array of memory cells] associated memory device, the method comprising [the following steps]:

selecting a first one of the memory devices;

transferring a first local address from a memory controller to the first memory device, with the first local address comprising at least three bits of address that are transferred to the first memory device over the system bus in parallel, wherein the first local address uniquely identifies the first memory device;

selecting a second one of the memory devices;

transferring a second local address from the memory controller to the second memory device, with the second local address comprising at least three bits of address that are transferred to the second memory device over the system bus in parallel, wherein the second local address uniquely identifies the second memory device;

selecting a third one of the memory devices; and

transferring a third local address from the memory controller to the third memory device, with the third local address comprising at least three bits of address that are transferred to the third memory device over the system in parallel, wherein the third local address uniquely identifies the third memory device.

55. The method of claim 47 including selecting one of the memory devices, subsequent to transferring local addresses to the memory devices, by transferring a select command over the system bus containing an address that corresponds the local address transferred to the memory device to be selected, switching the memory device to be selected to a device-enabled state in response to receipt of the select command.

56. The method of claim 55, further including performing a memory read operation on the memory device in the device-enable state.

57. The method of claim 56, further including switching the memory device in the device-enabled state to a device-disabled state by transferring a deselect command to the memory device to be switched, said deselect command containing an address which corresponds to the local address transferred to the memory device to be switched to the device-disabled state.

58. (Once amended) A memory system comprising:

a plurality of separate memory devices, with each of the memory devices comprising:

(a) an array of memory cells;

(b) an addressing circuitry [adapted to address] operatively coupled to the array of memory cells, wherein the addressing circuitry is capable of providing addresses to the array of the memory cells;

(c) a memory device bus interface;

(d) a command decoder which decodes commands at the memory device bus interface, including an address assign command; [and]

(e) a local address storage circuitry which stores a local address [for] identifying the storage circuitry's single [the] associated memory device once the address assign command is decoded by the command decoder;

(f) a lockout circuit switchable between a lockout state and a non-lockout state;

[(f)] (g) a select signal input and a select signal output, with the select signal output being active when both the select signal input is active and the lockout circuit is in the non-lockout state; and

a memory controller having a controller bus interface coupled to the memory device bus interface of each of the memory devices, with the memory controller having a select signal output connected to the select signal input of at least one of the memory devices and providing the local address uniquely identifying each of the memory devices.

59. The memory system of claim 58, wherein the memory controller has a separate select output connected to the select signal input of each of the memory devices so that the memory controller can select one of the memory devices by causing the select signal output connected to the memory device to be selected to become active.

61. The memory system of claim 58, wherein the memory controller is configured to provide a plurality of separate select signal outputs and wherein the separate memory devices are arranged in a plurality of banks, with each bank comprising a plurality of memory devices, with a first one of the memory devices of each of the banks having a separate select signal input connected to a separate one of the select signal outputs of the memory controller.

REMARKS

The Examiner is invited to contact the below-signed attorney to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

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